EE2026 (Part 1)
Tutorial 3 - Questions

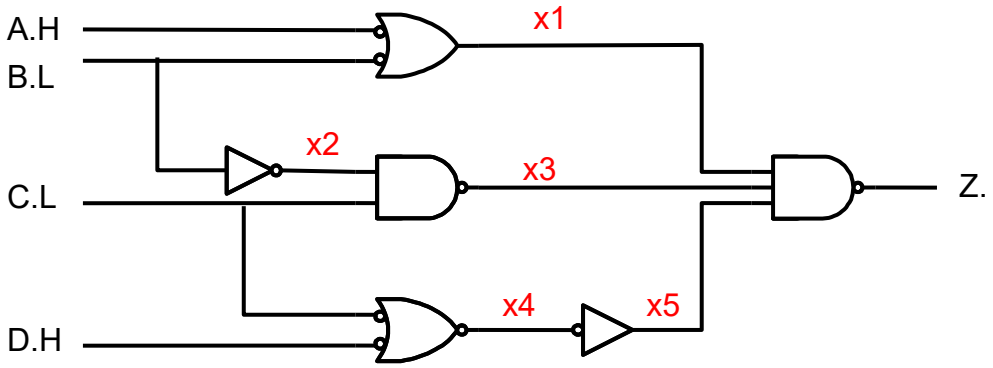
Logic gates

1. Use algebraic manipulation to find the MSOP for $f = x_1x_3 + x_1\overline{x_2} + \overline{x_1}x_2x_3 + \overline{x_1}\,\overline{x_2}\,\overline{x_3}$.
   Write the Verilog code that describes the above function as a module (use dataflow description style).

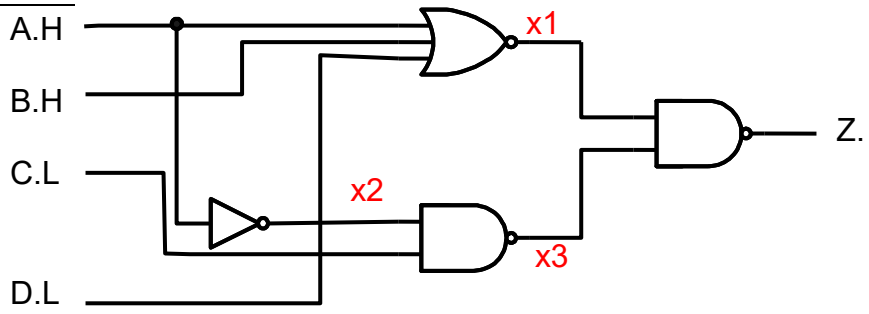
2. For circuits 1 and 2 below:

   (a) Fill in all the intermediate signal names using the positive logic convention
   (b) Find the logic expression for *Z* for the two cases
   (c) Write the Verilog code that describes the above function as a module (use structural description style). In the description, assume that only the Verilog primitives are available (no need to describe): not(out,in), nand(out,in1,in2,...), nor(out,in1,in2,...).

Circuit 1



Circuit 2



3. Design a logic circuit implementing the following Boolean function, using only NOR gates:

$$X = A \oplus B \oplus C$$

where $\oplus$ represents the 2-operand XOR operation. Use alternate gate representation if necessary for clear circuit diagrams.
Write the Verilog code that describes the above function as a module (use dataflow description style).

4. Design a circuit to realize $Z = \overline{A}B + \overline{B}\overline{C}D + \overline{B}\overline{D}$ in the positive logic convention. A and B are active low signals while C, D and Z are active high. Use a minimum number of gates, and draw clear circuit diagrams with alternate gate representations as required.
Write the Verilog code that describes the above function as a module (use dataflow description style).